A COMPARISON BETWEEN ACTIVELY AND PASSIVELY MATCHED S-BAND GaAs MONOLITHIC FET AMPLIFIERS

Raymond S. Pengelly, James R. Suffolk, John R. Cockrill and James A. Turner
Plessey Research (Caswell) Limited,
Allen Clark Research Centre,
Caswell, Towcester, Northants.
Telephone No. (0327)50581

ABSTRACT

The ability to design monolithic GaAs circuits which are insensitive to active and passive component variations is demonstrated. Actively and passively matched monolithic S-band amplifiers are compared in terms of reproducibility, GaAs usage, power consumption and processing complexity.

INTRODUCTION

The requirements of low cost monolithic GaAs circuits for certain systems such as phased arrays result in designs which are a compromise between performance, GaAs area usage, power consumption and overall yield. For multifunction chips it is clear that the sensitivity of circuit performance to processing, material parameters, design accuracy and repeatability is important.

The design of monolithic low noise receiver front-ends has shown that, with careful consideration in the use of GaAs FETs and passive components, circuits can be designed which are much more tolerant of component variations from batch to batch and the absolute accuracy of those components in circuit realisations than in other circuits which produce similar performance.

Two design examples are presented which offer two solutions to a monolithic broadband low noise amplifier circuit at S-band. The extent to which these circuits meet certain requirements is measured in terms of the sensitivities of reflection coefficient, gain flatness and noise figure to on-chip passive component and GaAs FET S-parameter variations. Such sensitivities determine the variation that will be seen from batch to batch. Also the sensitivity of the circuits to prime component values and parasitic component values is assessed. The monolithic GaAs FET preamplifier forms part of a complete S-band image rejection receiver front end covering the frequency range 2.7 to 3.5 GHz to be realised on a GaAs chip approximately 6 mm square.

MONOLITHIC CIRCUIT DESIGN PRINCIPLES

The first solution consists of a passively matched preamplifier using a sub micron gate length FET. The circuit diagram is shown in Fig. 1 the circuit producing a gain of 9 dB with a 3 dB noise figure, where the FET is stabilised using resistive loading, rather than inductive loading in the source of the FET, the former technique leading to a circuit which is less sensitive to matching component variations. The circuit shown in Fig. 2 consumes 50 mW power and operates from a 5 volt supply. The IC measures 3.5 to 4.5 mm. As may be seen from Fig. 2 the GaAs IC uses a considerable number of passive matching components to produce flat gain over the operating frequency range. Hence the Q values of the lumped elements used need to be as high as is feasible to minimise the effect of their loss on gain and noise figure. At S band most inductors are produced using multiturn spirals which use 15μm wide conductors (assuming a 150μm thick GaAs chip with a ground plane on its backside). Since the IC was designed initially to use VPE material a number of 'select-on-test' bias resistors are required (to enable the device to be operated at approximately 15% I_{DSS} for low noise operation) where the variation in I_{DSS} and pinch-off voltage, V_p are of known distribution over a GaAs wafer.

The performance of such a circuit is shown in Figs. 3(a),(b) and (c). The input VSWR is not particularly low because the device is matched for noise figure in a common source configuration. Figs. 4(a), (b) show the results of a Monte Carlo sensitivity analysis on the circuit of Fig. 1, where the components are varied by up to ± 10% in all their values in a normally distributed fashion. From these figures it may be expected that the variation in gain of the chip design with random variations in component values will be of the order of ± 1.3 dB (standard deviation about the mean value of 8.7 dB at 2.7 GHz). In reality it is likely that major component variations will be systematic - for example, resistors will be either all high or low in value due to the resistivity of the films being incorrect. For example (from Figs. 3(a)), if all the interdigital capacitors are calculated to be 20% too low in value there will be a reduction of 1 dB in gain over that expected. More importantly if element values are calculated incorrectly (either due to the use of incorrect formulae or component equivalent circuit models failing in accuracy) the circuit response will be affected. For example, if all inductors are calculated to be 50% lower in value than later measurements confirm, Fig. 3(c), for example, predicts that the noise figure will increase to over 9 dB at 3.5 GHz as against the nominal value of 3 dB. Obviously such discrepancies are unlikely but accuracies to within 10 to 15% are normal for spiral inductors, for example, when using the formulae of Grover or Greenhouse[1,2]. Thus, such changes in performance are excellent indicators of the circuit sensitivity.

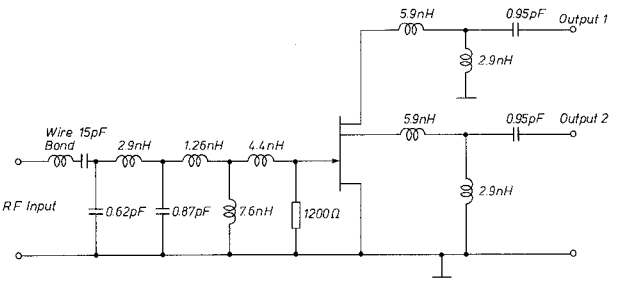

FIGURE 1: CIRCUIT DIAGRAM OF LOW NOISE PASSIVELY MATCHED SPLITTER AMPLIFIER. Note: Bias components not shown. Intrinsic circuit elements shown only.

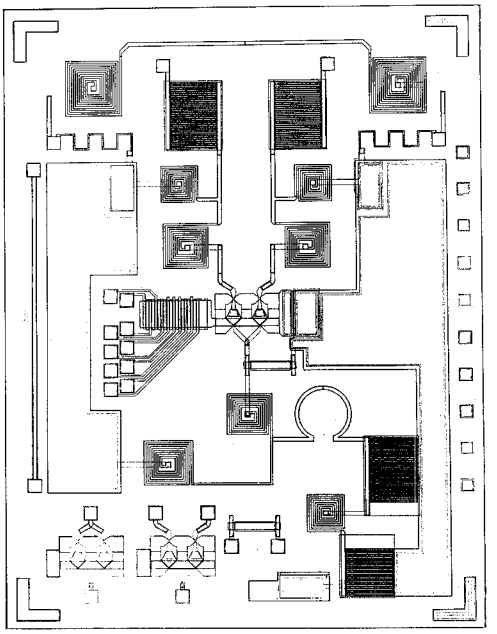

FIGURE 2: DESIGN OF MONOLITHIC GaAs PASSIVELY MATCHED LOW NOISE SPLITTING AMPLIFIER

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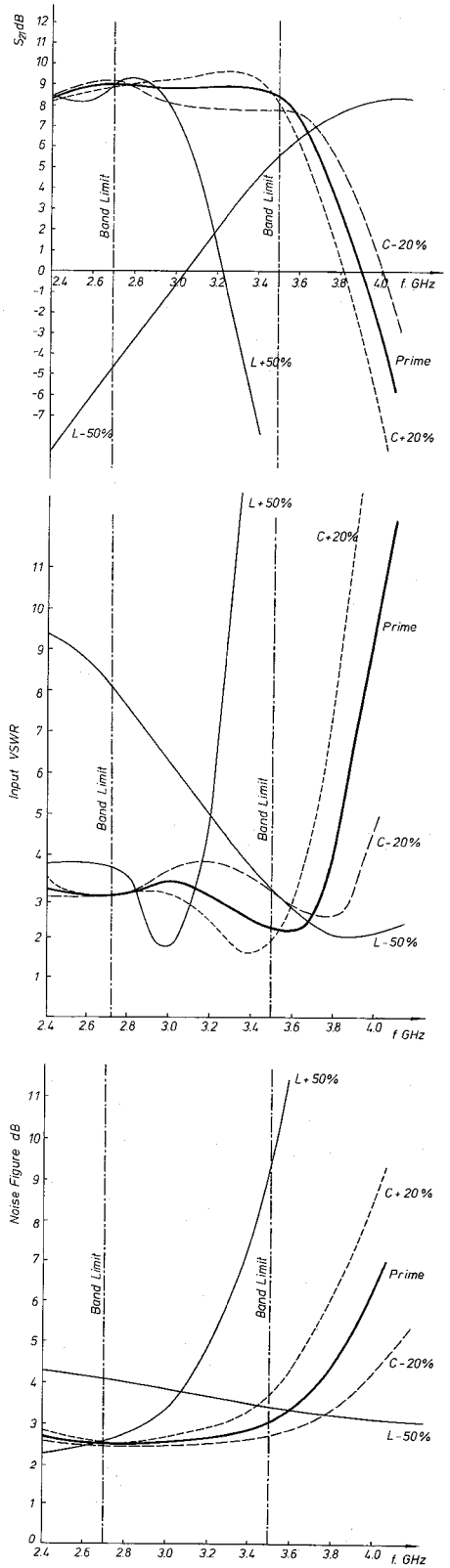

FIGURE 3: PERFORMANCE OF PASSIVELY MATCHED LOW NOISE AMPLIFIER (a) VARIATION OF GAIN, (b) VARIATION OF INPUT VSWR, (c) VARIATION OF NOISE FIGURE

The second circuit design shown in Fig. 5 uses a common gate, common source, source-follower cascade to produce a low noise preamplifier. The common gate input stage provides an almost simultaneous power gain and noise figure match for a FET having a 20 mS transconductance. Although the noise figure and associated gain of a common gate stage are higher and lower respectively than a common source stage a low I/P VSWR can be achieved over wide bandwidths without the need for balanced stages.

The FETs used, like the circuit of Fig. 2, employ submicron gate lengths. The chip realisation is shown in Fig. 6 where the GaAs IC is 2.2 mm by 3 mm. This circuit produces 19 dB gain over the 2 to 4 GHz frequency range with a noise figure of <4 dB over the 2.7 to 3.5 GHz band.

Applying the same Monte Carlo sensitivity analysis as in the first design, indicates that this preamplifier is three times less sensitive to component value changes, even though there are more FETs, resistors etc. Fig. 7(a),(b),(c) show the gain, input VSWR and noise figure change with $\pm$ 50% changes in inductors and $\pm$ 20% changes in capacitors. As may be seen the design is virtually insensitive to capacitance changes of this order and indeed the $|S_{21}|$ and $|S_{11}|$ are much more 'well behaved' where in fact a 50% decrease in inductance only decreases the gain by 2 dB in the 2.7 to 3.5 GHz band. Noise figure is also relatively well behaved for inductance values decreases from the optimised values by 50%.

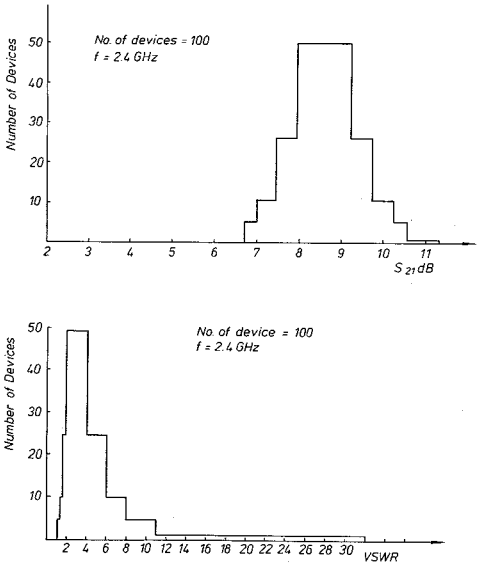

FIGURE 4a,b: MONTE CARLO RESULTS FOR PASSIVELY MATCHED LOW NOISE SPLITTER AMPLIFIER

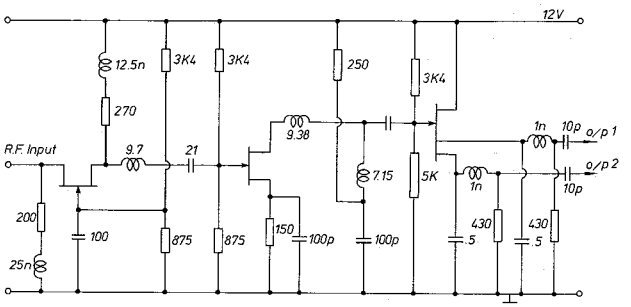

FIGURE 5: CIRCUIT DIAGRAM OF LOW NOISE ACTIVELY MATCHED SPLITTER AMPLIFIER

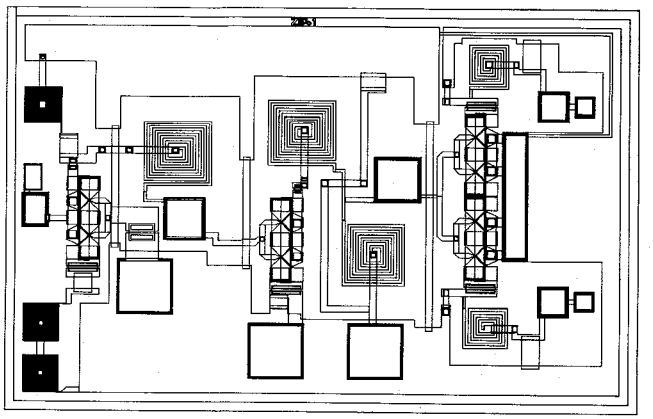

FIGURE 6: DESIGN OF A MONOLITHIC GaAs ACTIVELY MATCHED LOW NOISE SPLITTING AMPLIFIER

Thus, the actively matched solution appears to offer a design which, with expected ± 10% variations in component parameters, will produce a monolithic circuit with high reproducibility. The use of implanted material also means that I_{DSS} and V_p variations will be considerably smaller than for a smaller VPE wafer, thus lowering the cost of the complete IC.

For the case of likely variations in component values, based on measurements made using test structures, prime element values are known to within 15%. Such variations in capacitor, resistor and inductor values in Fig. 6 show that the circuit is well behaved with acceptable performance variations.

So far, the effect of variations in the parasitic elements associated with the lumped components has been neglected. Extensive measurements on such components has shown that the paraditic elements can be predicted to within 30%. Thus, the circuit of Fig. 6 has been assessed in its performance from the viewpoint of changing the parasitics from the values used for circuit design (which are actually those found by fitting the equivalent circuit models of the component to their measured S-parameters) by ± 30%.

Fig. 8(a) shows a mean gain value of 17.75 dB over the 2.7 to 3.5 GHz frequency range which is a worst case value for probable compnent value errors and loss. If all the parasitic capacitances are varied by ± 30% a worst cade variation in gain of ± 1 dB is observed.

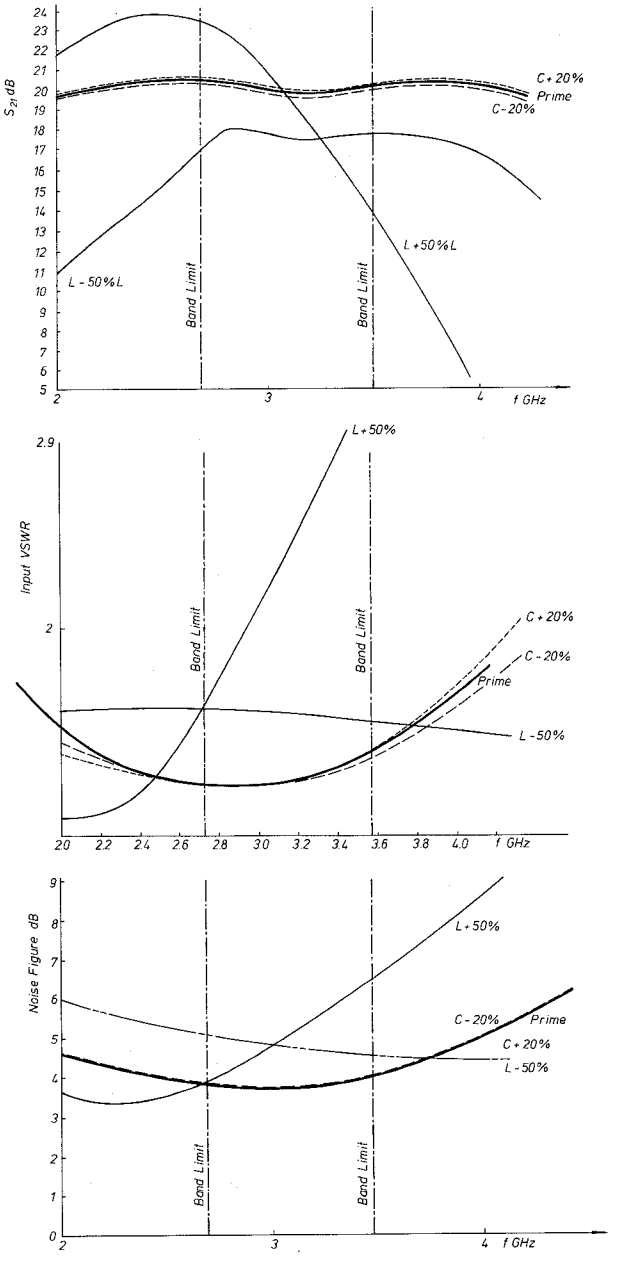

FIGURE 7: PERFORMANCE OF ACTIVELY MATCHED LOW NOISE SPLITTER AMPLIFIER, (a) VARIATION OF S_{21} WITH MATCHING COMPONENT CHANGE, (b) VARIATION OF INPUT VSWR WITH MATCHING COMPONENT CHANGES, (c) VARIATION OF NOISE FIGURE WITH MATCHING COMPONENT CHANGE

Fig. 8(b) and (c) show, respectively, the variation in noise figure and input VSWR for the case where the active and passive component values are set for the expected worse case performance and the parasitic elements are varied by ± 30%.

The actively matched solution, uses approximately 480 mW of d.c. power, with a 12 volt supply rail because of the utilization of resistive loading of the FETs rather than r.f. chokes.

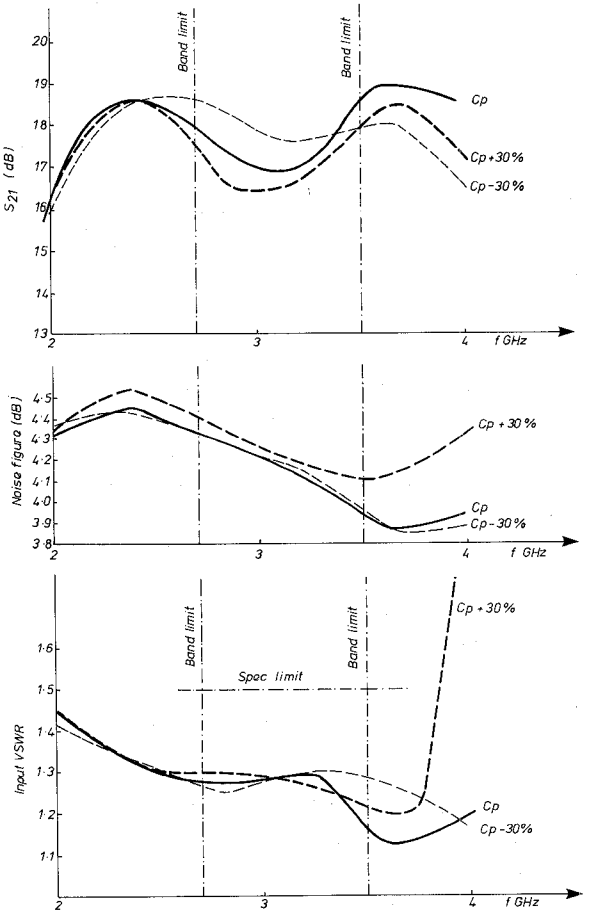

FIGURE 8(a) VARIATION OF S_{21} WITH PARASITIC ELEMENT CHANGES, (b) VARIATION OF NOISE FIGURE WITH PARASITIC ELEMENT CHANGES, (c) VARIATION OF INPUT VSWR WITH PARASITIC ELEMENT CHANGES

CONCLUSIONS

In conclusion it has been shown that by the use of actively matched GaAs FET configurations with simple d.c. blocking and simple r.f. matching components, S-band low noise monolithic amplifiers can be realised using half the GaAs area compared to that of a passively matched solution. The resultant design is less likely to depart from the optimised performance when compared to the passively matched circuit considering likely processing tolerances, prime element value accuracy and parasitic element value accuracy. In order to maintain the noise figure performance of the smaller chip, a supply voltage of greater than 10 volts has been chosen.

Further examples of such GaAs monolithic circuits including active splitters, actively matched FET mixers, IF processing circuits etc., have led to an overall receiver design which is capable of being produced on a single chip of GaAs with a low sensitivity to component and bias variations (due to likely processing and material changes and absolute component values).

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